ABSTRACT OF THE DISCLOSURE

In a nonvolatile memory array in which each cell (110) has two floating gates (160), for any two consecutive memory cells, one source/drain region (174) of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the appropriate conductivity type (e.g. N type) formed in a semiconductor substrate (120). Each such contiguous region provides source/drain regions to only two of the memory cells in that column. The bitlines (180) overlie the semiconductor substrate in which the source/drain regions are formed. The bitlines are connected to the source/drain regions.